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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,277	07/23/2003	Dong-Sauk Kim	29926/39495	8394

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,277	KIM ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11, 13-17 and 19-24* is/are allowed.

6)☒ Claim(s) *1-6, 12 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (figure 4) in view of Kaeriyama (U.S. 6,150,214).

As to claims 1 and 12, the admitted prior art (figure 4) discloses a semiconductor device and a corresponding method, comprising: a plurality of capacitor plugs (41) formed within a predetermined interval interleaved between two bit lines (40) and midpoints of capacitor plugs (41) are located at inter-section points of X axis virtual line (X1, X2) and Y axis virtual line (Y1, Y2), wherein the X axis virtual lines (X1, X2) are parallel with the bit lines (40) and the Y axis virtual lines (Y1, Y2) are perpendicular to the X axis virtual lines (X1, X2); and a plurality of lower electrodes (42, 42A, 42B) of capacitors formed within a predetermined interval to be respectively connected with the capacitor plugs (41) in one to one correspondence.

The admitted prior art (figure 4) does not disclose each lower electrode is circularly shaped.

Kaeriyama discloses in figure 4 a semiconductor device wherein each lower electrode ("capacitor plate" 16) is circularly shaped. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of the admitted prior art (figure 4) by having each lower electrode which is circularly

shaped as taught by Kaeriyama for reducing the critical dimensions of active elements, thus increasing the functionality and performance of the semiconductor device (see col. 1, lines 20-31 in Kaeriyama).

As to claim 2, the admitted prior art (figure 4) discloses a semiconductor device, wherein a lower electrode (42) and neighbored lower electrode (42A) disposed along a direction of Y virtual axis line are formed not to have overlapped area, if one of lower electrode (42) is moved to same X virtual axis line as the other lower electrode (42A or 42B).

As to claim 3, the admitted prior art (figure 4) discloses a semiconductor device, wherein the lower electrode (42) and neighbored lower electrode (42A) disposed along a direction of Y virtual axis (Y1'', Y2'') are not on the same Y virtual axis (Y1'' and Y2'' are not on the same axis).

As to claim 4, the admitted prior art (figure 4) discloses a semiconductor device, wherein the midpoints of the lower electrode (42) and the neighbored lower electrode (42A) are not disposed along the same Y virtual axis (Y1'' and Y2'' are not on the same virtual axis).

As to claim 5, the admitted prior art (figure 4) discloses a semiconductor device, wherein a ratio of a major axis (X1, Y1''; and X1, Y1) to a minor axis (X1, Y2''; and X1, Y2) of the upper plane of the lower electrodes (42, 42A) ranges from about 1 to 1.

As to claim 6, the admitted prior art (figure 4) discloses a semiconductor device, wherein an area of an upper plane of the lower electrode (42, 42A) is practically identical to that of an lower plane of the lower electrode (lower electrodes 42B) in view of a three-dimensional structure and the lower electrode having a lateral plane (a lateral plane is the intermediate bit line 40 positioned between the upper and lower planes of the electrodes) which connects the upper

plane with the lower plane, wherein the lateral plane is substantially vertical to the upper plane and lower plane respectively.

The admitted prior art (figure 4) does not disclose and the lower electrode features a circular cylinder structure.

Kaeriyama discloses in figure 4 a semiconductor device wherein the lower electrode ("capacitor plate" 16) features a circular cylinder structure. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of the admitted prior art (figure 4) by having a lower electrode that features a circular cylinder structure as taught by Kaeriyama for reducing the critical dimensions of active elements, thus increasing the functionality and performance of the semiconductor device (see col. 1, lines 20-31 in Kaeriyama).

As to claim 18, the admitted prior art (figure 4) discloses a semiconductor device and a corresponding method, wherein an area of an upper plane of the lower electrode (42, 42A) is practically identical to that of an lower plane of the lower electrode (lower electrodes 42B) and the lower electrode having a lateral plane (a lateral plane is the intermediate bit line 40 positioned between the upper and lower planes of the electrodes) which connects the upper plane with the lower plane and practically vertical to the upper plane and lower plane.

The admitted prior art (figure 4) does not disclose and the lower electrode has a circular cylinder structure.

Kaeriyama discloses in figure 4 a semiconductor device wherein the lower electrode ("capacitor plate" 16) has a circular cylinder structure. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the

semiconductor device of the admitted prior art (figure 4) by having a lower electrode that has a circular cylinder structure as taught by Kaeriyama for reducing the critical dimensions of active elements, thus increasing the functionality and performance of the semiconductor device (see col. 1, lines 20-31 in Kaeriyama).

Allowable Subject Matter

3. Claims 7-11, 13-17 and 19-24 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter:

Claim 7 recites, inter alia, "a semiconductor device comprising a plurality of capacitor plugs; a plurality of lower electrodes of capacitors; and a plurality of contact pads are formed between the lower electrodes and the capacitor plugs, wherein the contact pads are formed over the capacitor plugs and disposed at a lower plane of at least one of the paired lower electrodes"; and in the combination with other claimed limitations.

Claim 13 recites, inter alia, "*a method for fabricating a semiconductor device comprising: a plurality of capacitor plugs; a plurality of lower electrodes of capacitors; depositing a sacrifice insulation layer over the capacitor plug formed over a semiconductor substrate; forming a plurality of open parts exposing the capacitor plugs by performing an selective etching of the sacrifice insulation layer by using a mask pattern; depositing a material for the lower electrode on an entire profile of the semiconductor substrate comprising the open parts; forming the lower electrodes separated from each other by performing a planerization process until the sacrifice insulation layer is exposed; and removing the sacrifice insulation layer by carrying out a wet dip-out process*"; and in the combination with other claimed limitations.

Claim 19 recites, inter alia, "a method for fabricating a semiconductor device comprising: a plurality of capacitor plugs; a plurality of lower electrodes of capacitors; a plurality of contact pads are respectively formed between the lower electrodes and the capacitor plugs after forming the capacitor plugs, wherein the contact pads serve as connecting the lower electrode with the capacitor plug electrically"; and in the combination with other claimed limitations.

The prior art of record does not teach or render obvious to modify the art of record so as to include the above mentioned-limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments filed 09/30/05 have been fully considered but they are not persuasive.

As to claims 1-6, 12 and 18, in pages 9-10, Applicant argued that Kaeriyama et al does not teach or suggest the plates 16, 18 are circularly-shaped lower electrodes.

In response, the examiner respectfully disagrees with Applicant about the issue. It is clearly shown in Fig. 4 of Kaeriyama that a semiconductor device wherein each lower electrode ("capacitor plate" 16) is circularly shaped. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of the admitted prior art (figure 4) by having each lower electrode which is circularly shaped as taught by Kaeriyama for reducing the critical dimensions of active elements, thus

increasing the functionality and performance of the semiconductor device (see col. 1, lines 20-31 in Kaeriyama).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

HOAI PHAM
PRIMARY EXAMINER